Smart Rack Monitor

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Introduction

This note describes the design of a general purpose data acquisition chassis based on the Motorola MC68332 microcontroller. The goal for this design is to provide a chassis that satisfies the data acquisition requirements for the Linac upgrade project and that can be placed in remote areas and provide some local processing near the data sources. Typical local processing tasks include local closed loop control, such as rf amplitude control, water temperature stabilization, linearizing the output from nonlinear sensors, stepping motor control, and implementing counters and predet timers.

General description

Figure 1 shows the block diagram of the Smart Rack Monitor (SRM). The overall arrangement of I/O is patterned after the DZero Rack Monitor. Similarities are the 64-channel differential A-D input, eight bytes of digital I/O and eight of D-A output channels. Major differences are; the addition of a Motorola MC68332 microcontroller, eight more D-A channels, the ability of each digital I/O bit to function as either input or output, the replacement of MIL-1553 with an Arcnet local area network and the provision for adding small custom I/O daughterboards. The SRM is packaged in a 2U (3.5 in.) rack mount chassis that has analog and digital I/O connectors on the lower 1U arranged in the same way as the DZero rack monitor, with additional connector space available on the upper part of the rear panel. A diagram of the SRM is shown in Figure 1.

The MC68332 Microcontroller

Motorola has recently introduced the MC68332, a 68020-based microcontroller that includes sixteen counter/timer channels, a serial communication interface, 2 kbytes of RAM and a system integration module. This processor is available as a small subsystem called a Business Card Computer (BCC), a 2.25 by 3.5 inch circuit board that has the MC68332, 128 kbytes of PROM, 64 kbytes of RAM and an RS-232 serial interface. The BCC attaches to the motherboard by the two 64-socket DIN connectors aligned along the long sides of circuit board as shown in Figure 1. All the address, data, control and I/O pins of the MC68332 are available on these two DIN connectors. Included on the silicon of the MC68332 is an extensive system integration module, a collection of interface features normally provided by peripheral circuits. The system integration module includes twelve programmable chip selects, interrupt and interrupt acknowledge circuits, a bus timeout timer, a programmable periodic interrupt clock, and a software watchdog timer. In addition to the memory included on the BCC, two 32-pin sockets are included on the motherboard to hold non-volatile RAM that can be used for either program or data storage.

Analog Input

Four connectors on the rear panel of the SRM are used to connect the analog inputs to eight 8-channel differential input multiplexers. Outputs from these multiplexers are combined by a ninth multiplexer that drives an instrumentation amplifier followed by the digitizer. The A-D converter is one of a family of digitizer chips supplied by Crystal Semiconductor. Pin compatible converters with twelve, fourteen or sixteen bit resolution may be used as required. Crystal A-Ds are CMOS devices that use a successive approximation charge redistribution digitizing technique and include an onboard microcontroller to recalibrate the device at power-on time or by external command. An input signal sample-and-hold function is inherent in the design of these converters. The MC68332 will directly control the input multiplexers and the A-D converter, so that in addition to the normal periodic scan of all analog input channels, special processing, such as repetitive reads of selected channels, would be possible.

Analog Output

Four Analog Devices AD664 quad D-A circuits are included in the SRM. The D-A registers appear as memory locations that can be read and set. Output ranges of these converters are programmable and ranges of ± 5V, 0-10V and ±10V may be selected. A read of the setting register returns the stored setting of selected D-A registers. The D-A settings are cleared to zero by a power-on reset, but a reset output by the processor will not clear the stored settings in the D-As.

Digital I/O

The SRM normally uses the 74ALS652 as its digital I/O chip, a non-inverting bidirectional octal latch-buffer circuit with high active totem pole outputs. All digital I/O lines are pulled to +5V with 1 kohm pullup resistors. At power up the latches are cleared to "0" setting all digital output pins to a TTL low state. A "1" written to a digital output bit will drive the corresponding pin high and read back as a "1". The data direction of the digital I/O is separately determined for each byte by a front panel piano DIP switch. A *Read* of an I/O byte returns the state of the pin, not the logic value stored in the latch. Digital I/O is accessible as bytes of memory so the software can interact with individual I/O bits using the processor's indivisible BSET and BCLR instructions. Two bytes of digital data are connected to each of the four 37-socket "D" connectors. Also included in each connector are two strobe signals to indicate a processor access to each of the two bytes, a buffered R/W line that gives the direction of the data transfer, and a +5V line that can be used to activate external opto isolators or small relays. Because each I/O bit is internally pulled up, external isolated contact closures can be sensed directly, without connection to the user's power or ground.

For special applications, other digital I/O chips may be used. The 74LS651,2,3 and 4 are a pin-compatible family of interface buffers that provide all combinations of inverting and non-inverting, totem pole and open collector outputs. Totem pole versions can sink 48 milliamps to a TTL low, and drive at least 15 milliamps to a TTL high.

Network Interface

The SRM connects to other modules and to the Local Station computer by an Arcnet local area network. This differs from the MIL-1553 connection used for the DZero rack monitor because that device did not include a processor. MIL-1553 can be used for non-intelligent devices; local area networks must terminate at computers.

Arcnet, although not an IEEE standard, still claims more installed nodes than either Ethernet or Token Ring. Part of Arcnet's popularity comes from its simplicity, low cost, ease of installation, and the multi-source availability of highly integrated support silicon. Interchangeable interface drivers are available for coax, twisted pair and fiber optic media. The SRM will use the standard transformer coupled coax medium, except for locations where high voltage electrical isolation is required, such as the Preaccelerator domes.

Arcnet uses a token bus protocol operating at a 2.5 MHz signalling rate; all stations on the network see the token when it is passed from one station to the next in increasing station address order. It is a physical bus and a logical ring. Because it is a peer protocol network, any node can initiate a transmission. Network reconfiguration occurs whenever a station enters or leaves the network, an operation that is accomplished entirely by the Arcnet controller chips themselves without intervention by the host processors.

Messages passed on an Arcnet network are protected by a sixteen bit CRC word and have a 508 byte maximum length. The transmitting station acquires the token, makes a "free buffer enquiry" of the intended receiving station, and upon receiving a positive acknowledge, sends the message. The destination station returns either a positive or a negative acknowledge so the transmitting station knows immediately if the message was received without errors. All of the protocol described here is handled by the Arcnet controller chips. The host computer simply places the message in the Arcnet chip's buffer and sets a control register bit to indicate that the message should be transmitted. On the destination end, the host processor may be interrupted when a message has been successfully received.

I/O Daughterboard

To satisfy the need for custom interfaces, provision is made to add small daughterboards to the SRM motherboard. These daugh-

terboards have the same footprint and pinout as the Motorola BCC module so that all the facilities of the computer are available to the custom board. The motherboard has patterns for two additional BCC-pinout modules as shown in Figure 1. Features added to the SRM by the use of daughterboards can be connected to external equipment using connectors mounted in the upper half of the rear panel.

Counter/Timer I/O

The MC68332 microcontroller was originally designed for automotive engine control applications, so a time processing microengine is included on the silicon. The time processor includes several preprogrammed timing functions such as input transition counting, input capture and output compare timing, pulse period measurement, pulse width modulation, and stepper motor control. Any of the counter/time channels can cause an interrupt to the processor.

Because timing requirements vary from one project to another, the timer/counter interface for the Linac will be provided on a daughterboard. Included on this board will be a Tevatron or TAXI clock receiver, a buffered clock output, a few transformer coupled predet outputs, some counter input channels, and several uncommitted timer/counter channels.

The features of the MC68332 time processor can be used in the Linac system to implement local predet triggers and to count pulse inputs such as radiation detectors and klystron spark indicator pulses. Counter/ timer channels can appear to the Local Station as more analog channels and as such they may be read, set, named, monitored and alarmed on, just as any other analog channel.

Packaging

The SRM is packaged in a self-powered 2U (3.5 in.) rack mount chassis and all I/O is attached using socket type "D" connectors mounted to the rear panel. Diagrams of the mechanical outline and the placement of connectors is given in Figures 2 and 3. Pinouts of the A-D, D-A, and digital I/O connectors are included in Figures 4a, 4b, and 4c, respectively.

Software

Although the software for the SRM is only now being developed, it is planned that a subset of the present Local Station software including the pSOS real time kernel will be used. The network layer and the driver to read and set analog and digital parameters will be provided along with a provision to monitor the operation of a selected SRM from its Local Station. The architecture of this system should allow additional tasks to be downloaded to the SRM from the Local Station to accommodate custom control functions. In the case of the Linac control system, closed loops for the cavity temperature regulation, cavity gradient stabilization, and ion source pressure control will be run from the local SRM.

To monitor the operation of the SRM and to easily allow changing the mode of the system, a group of eight LEDs and eight sense switches are mounted on the motherboard for front panel access. These lights and switches are addressed as two bytes of processor memory.

Address and Chip Select Assignments

The MC68332 has twelve pins allocated for chip selects including *csboot* , the chip select that addresses the 128 kbyte PROM on the BCC board. Of the twelve available chip selects, three are used on the BCC, two for the non-volatile RAM, and one each for Arcnet, analog I/O, and digital I/O thus leaving three uncommitted chip selects available for use by the optional daughterboards. Each chip select is programmed to specify its base address, address range, data width, address space type, and timing characteristics. Because of the dynamic bus sizing feature of the 68020 style bus, the processor may read and write words and long words to a byte-wide port connected to data lines D15-D8.

Chip select and address space assignments are listed in Tables 1 and 2. Figure 5 is included to show the physical location of interface data in the rear panel "D" connectors.

Interrupts
Two interrupts may be asserted by onboard devices:

Level 3 - ARCNET Interrupt
Level 5 - A/D Interrupt

Other interrupts can be accessed by optional daughterboards as needed.

Current Status
Design of the Smart Rack Monitor is complete and the prototype board has been assembled and tested. Using interim software an Motorola's 332Bug pmonitor program, the prototype has been checked out and funtions as described here. Artwork has been corrected and the second pass pc boards have been requisitioned.

Chip Select	Device Selected	Base Address	Memory Range	Data Direction	U/L Byte
csBoot	BCC PROM	$60000	$20000	Read	U&L
cs0	BCC RAM0 Write	$000000	$10000	Write	U
cs1	BCC RAM1 Write	$000000	$10000	Write	L
cs2	BCC RAM Read	$000000	$10000	Read	U&L
cs3	Unassigned				
cs4	Digital I/O	$FF8000	$800	Read/Write	U
cs5	Analog I/O	$FF8800	$800	Read/Write	U & L
cs6	Arcnet	$FA0000	$1000	Read/Write	U
cs7	NonVolatile RAM	$10000	$10000	Read/Write	U
cs8	NonVolatile RAM	$10000	$10000	Read/Write	L
cs9	Unassigned				
cs10	Unassigned				

Table 1. Chip Select and Address Assignments

Address	Register	Data Direction
$FA0000	Arcnet RAM	Read/Write
$FA0800	Arcnet Registers	Read/Write
$FF8000	I/O Byte # 0	Read/Write
$FF8001	I/O Byte # 1	Read/Write
$FF8002	I/O Byte # 2	Read/Write
$FF8003	I/O Byte # 3	Read/Write
$FF8004	I/O Byte # 4	Read/Write
$FF8005	I/O Byte # 5	Read/Write
$FF8006	I/O Byte # 6	Read/Write
$FF8007	I/O Byte # 7	Read/Write
$FF8008	Program LEDs	Read/Write
$FF8009	Program Sw.	Read
$FF800A	Data Dir Switch	Read
$FF8800	DA0 Control Reg	Read/Write
$FF8808	DA0-0 Setting	Read/Write
$FF880A	DA0-1 Setting	Read/Write
$FF880C	DA0-2 Setting	Read/Write
$FF880E	DA0-3 Setting	Read/Write
$FF8810	DA1 Control Reg	Read/Write
$FF8818	DA1-0 Setting	Read/Write
$FF881A	DA1-1 Setting	Read/Write
$FF881C	DA1-2 Setting	Read/Write
$FF881E	DA1-3 Setting	Read/Write
$FF8820	DA2 Control Reg	Read/Write
$FF8828	DA2-0 Setting	Read/Write
$FF882A	DA2-1 Setting	Read/Write
$FF882C	DA2-2 Setting	Read/Write
$FF882E	DA2-3 Setting	Read/Write
$FF8830	DA3 Control Reg	Read/Write
$FF8838	DA3-0 Setting	Read/Write
$FF883A	DA3-1 Setting	Read/Write
$FF883C	DA3-2 Setting	Read/Write
$FF883E	DA3-3 Setting	Read/Write
$FF8840	A-D Status	Read
$FF8842	A-D Data	Read
$FF8844	Digitize Command	Write
$FF8847	Mux Chan Sel	Read/Write
$FF8848	A-D Calibrate	Write

Table 2. I/O and Digitizer Address Assignments

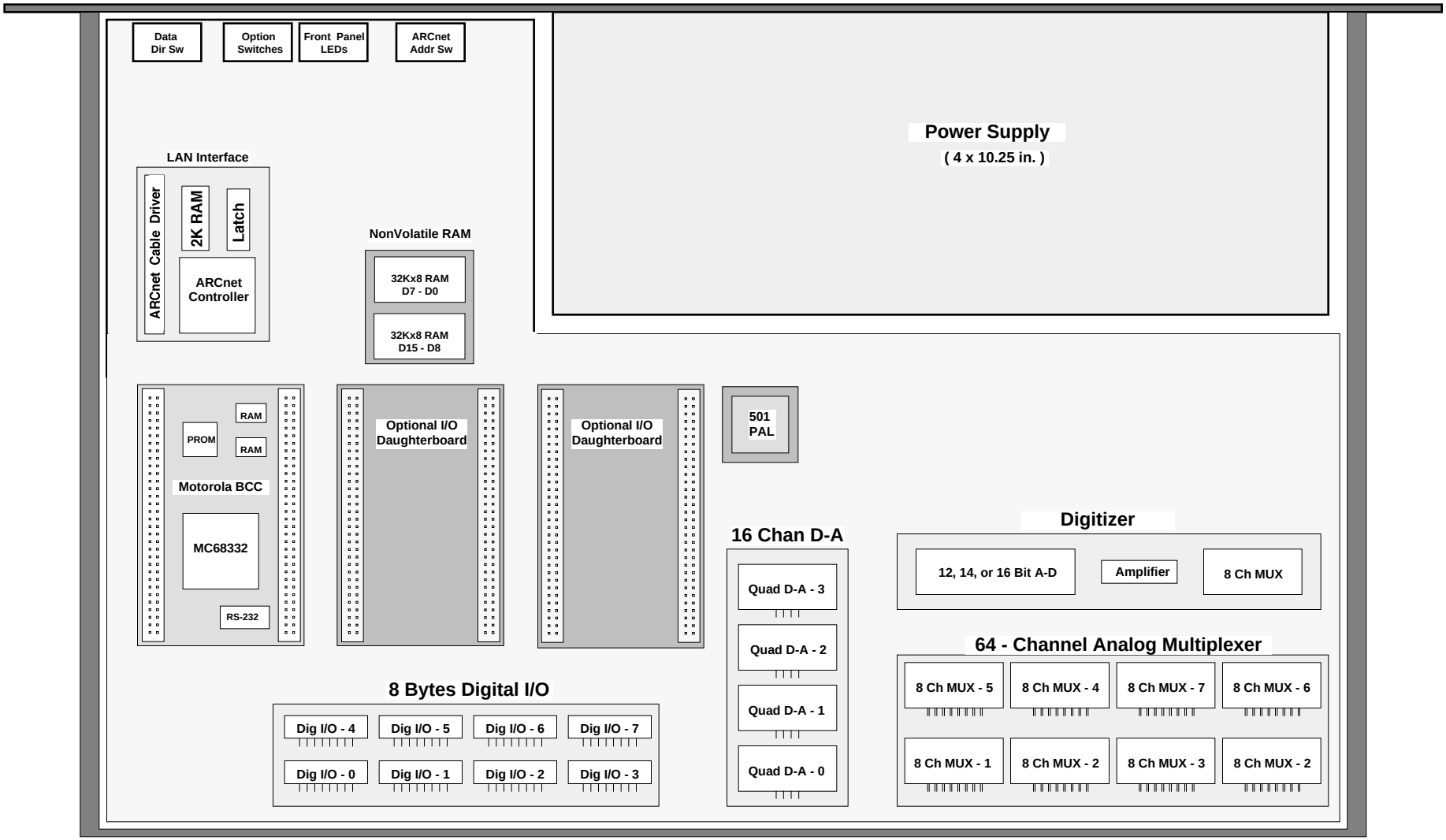

Figure 1. Smart Rack Monitor Block Diagram

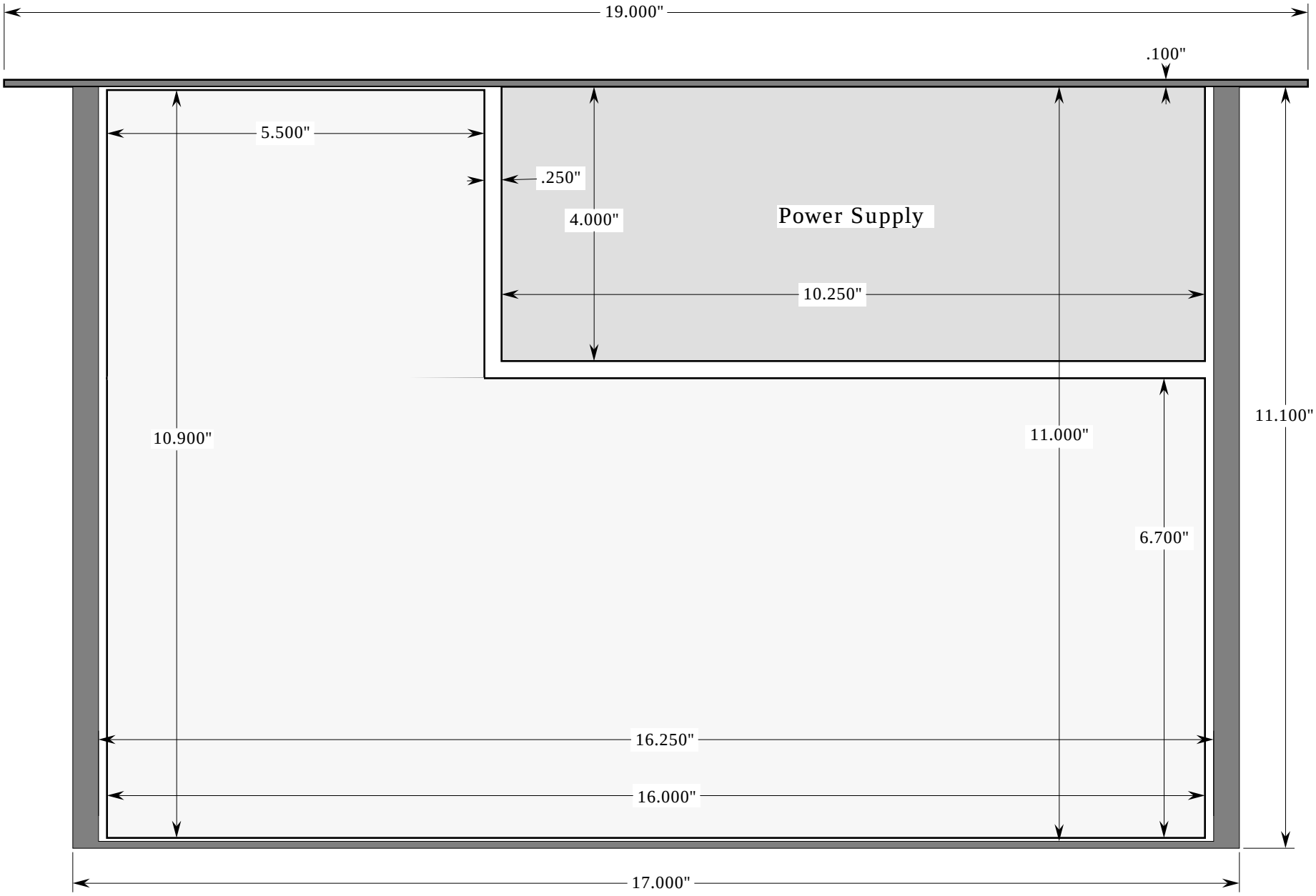

Figure 2. Smart Rack Monitor Mechanical Outline

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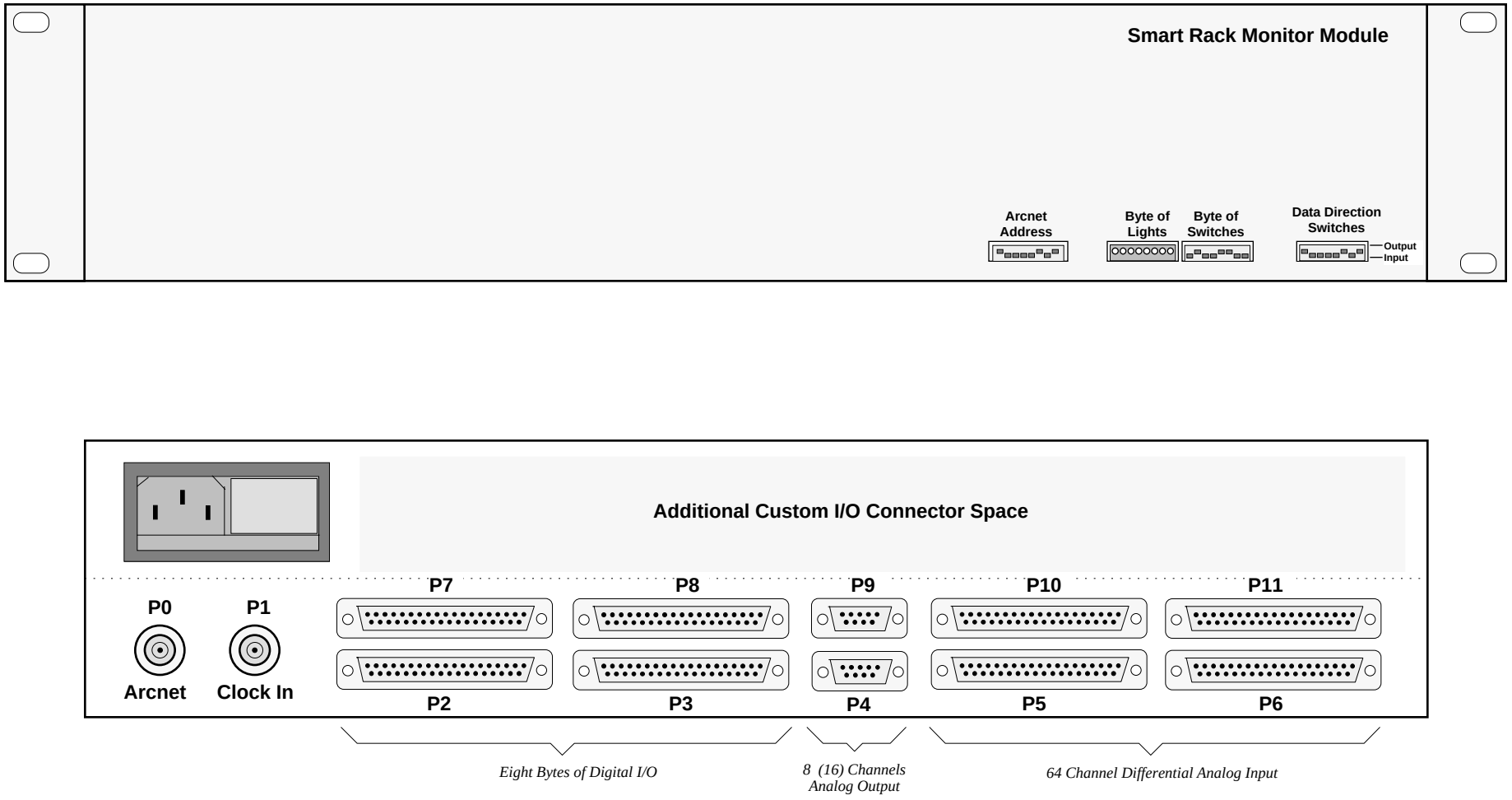
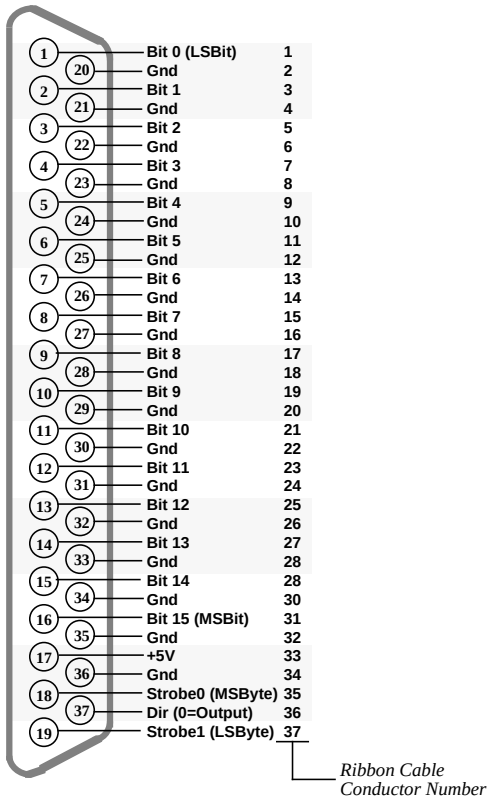


Figure 3. Smart Rack Monitor Front and Rear Panel Diagram



Note: Strobes are short positive pulses. Output data is valid on the trailing (high to low) transition of the strobe pulse.

Figure 4c. Digital Output P2, P3, P7, and P8

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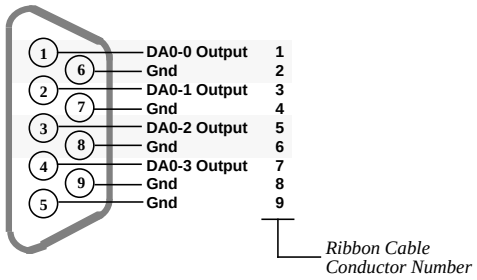
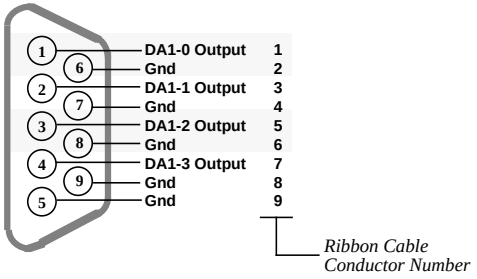


Connector P4



Connector P9

Figure 4b. DA Output

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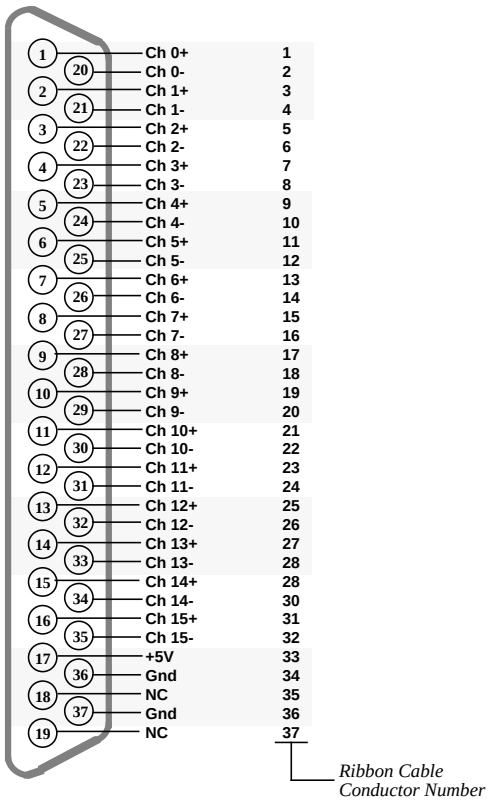

Note: +5V on Pins 17 is optional

Figure 4a. Analog Input Connector P5, P6, P10, P11

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Figure 4. Smart Rack Monitor Connector Pinouts

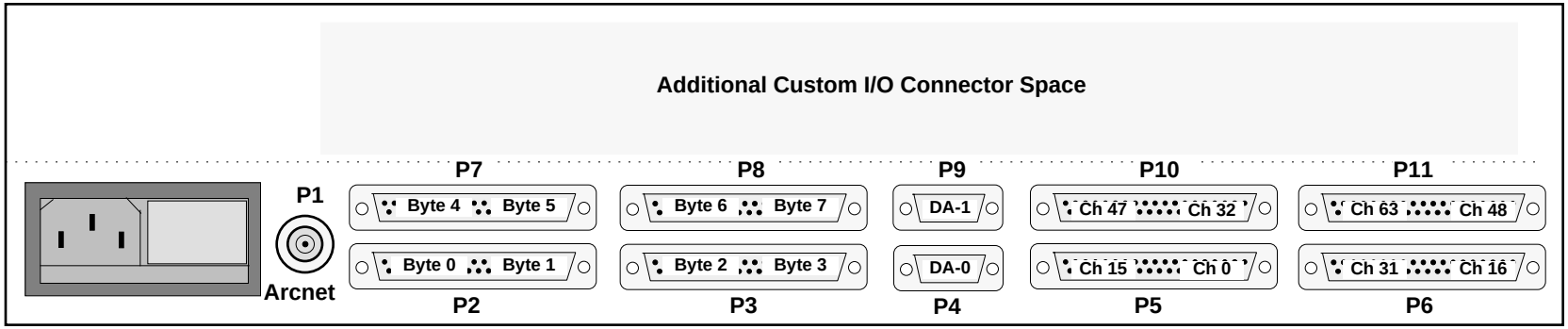

Figure 5. Smart Rack Monitor Data Physical Location

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